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Ta/Si Schottky diodes fabricated by magnetron sputtering technique

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ABSTRACT

Electrical properties of Ta/*n*-Si and Ta/*p*-Si Schottky barrier diodes obtained by sputtering of tantalum (Ta) metal on semiconductors have been investigated. The characteristic parameters of these contacts like barrier height, ideality factor and series resistance have been calculated using current voltage (*I–V*) measurements. It has seen that the diodes have ideality factors more than unity and the sum of their barrier heights is 1.21 eV which is higher than the band gap of the silicon (1.12 eV). The results have been attributed the effects of inhomogeneities at the interface of the devices and native oxide layer. In addition, the barrier height values determined using capacitance–voltage (*C–V*) measurements have been compared the ones obtained from *I–V* measurements. It has seen that the interface states have strong effects on electrical properties of the diodes such as *C–V* and R_s–*V* measurements.

1. Introduction

Metal semiconductor (MS) Schottky rectifiers have a great role in power supply industry over years because of their very low forward voltage drop and switching speeds. They are also the basis of a large number of semiconductor electronic devices including microwave diodes, field-effect transistors (FETs), solar cells and photo-detectors. The characteristic parameters of Schottky diodes are affected by interface quality between metal and semiconductor [1]. It is well known that except for special fabrication, all MS devices have a thin oxide interface layer and this layer converts the MS devices to metal–insulator–semiconductor (MIS) diodes [2–4]. Therefore, the interface oxide layer at MS rectifying contacts has a crucial role in determination of Schottky diode parameters such as the barrier height, the ideality factor and the series resistance [5–8]. The understanding of the detailed mechanisms of the oxidation, reduction and etching processes involved in wafer cleaning is essential for high device yield. Moreover, after the device fabrication, its performance and stability depending on time is an important matter in the device manufacturing [1–4]. Most Schottky diodes suffer from the presence of a thin insulating layer at the metal semiconductor interface, unless it is fabricated in the vacuum, and generally, an interface layer suppose of thickness 10–30 Å [1–5].

Sputter deposition of metallic films is one of the widely used techniques for microelectronic applications [9]. Especially, it is a practical way to deposit refractory metals. Sputter deposition involves the bombardment of a target with positive gas ions and leads to the bombardment of the growing film by energetic particles [9]. It is well known that metallization procedures such as sputtering and electron beam deposition introduce defects at and close to the metal–semiconductor junction [10]. Auret et al. have found that sputter deposition introduces several electrically active defects near the surface of Ge which have also been observed after high energy electron irradiation [10]. The defects formed during sputtering process effect the performance of the devices and change the barrier height of contacts [11,12]. Depending on the application, formed defects during the sputtering process may either be beneficial or detrimental for device performance. Sawko and Bartko [13] have showed that the defects introduced during high energy electron and proton irradiation increase the switching speed of Si based devices.

In this study, Ta/Si Schottky diodes have been fabricated by dc sputtering of tantalum on *p*-Si and *n*-Si wafers. The *I–V* and *C–V* measurements of diodes have been executed to determine their electrical parameters. In addition, the effects of interfaces states caused have been observed in *C–V* and series resistance (R_s) measurements at different frequencies. It has been stated [1–4,14,15] that localized electronic states with energies inside the band gap

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exist due to the termination of the periodic structure of the crystal lattice at the surface. Simply stated, the surface states can be viewed as electronic states generated by unsaturated dangling of the surface atoms. In the laboratory environment, crystal surfaces are usually covered with layers of native oxides and organic contaminations, and surface states in the presence of these layers are modified and referred to as 'interface states'. On the semiconductor surface, the presence of the surface states in the band gap is known to 'pin' the Fermi level position of the semiconductor.

2. Experimental procedures

The Ta/Si Schottky barrier diodes were prepared using one side polished *n*-Si and *p*-Si wafers with (1 0 0) orientation and 1–10 Ω cm resistivity. Before formation of structures, both wafers were boiled 3-chloroethylene and rinsed in acetone and isopropanol by ultrasonic vibration for 5 min to remove organic contaminations. They were immersed into solution of H_2O/HF (10:1) for 30 sn in order to remove native oxide layers on the surfaces and form H terminated surfaces. Preceding each step, the wafers were rinsed in 18 MΩ deionized water. After cleaning procedures, the wafers were dried under N_2 atmosphere and inserted into the vacuum chamber. Au and Al were sputtered on the unpolished side of *n*-Si and *p*-Si substrates, respectively, to make back contacts. The thicknesses of metals were measured as 250 nm via thickness monitor of the vacuum system during sputtering processes. Both structures were annealed at 450 °C in flowing N_2 in a quartz tube furnace. After formation of ohmic back contacts, the native oxide layers formed during previous processes were removed by solution of H_2O/HF (10:1) and dried under N_2 atmosphere. Both structures were simultaneously inserted into a vacuum system. Ta/*n*-Si/Au and Ta/*p*-Si/Al Schottky rectifiers were formed by sputtering of Ta on Si substrates. The diode diameters were 1.5 mm. The *I*–*V* measurements of the diodes were performed by Keithley 2400 sourcemeter in dark and the *C*–*V* measurements of the devices were performed using Agilent HP 4294A impedance analyzer (40 Hz–110 MHz) at room temperature.

3. Results and discussion

The *I*–*V* measurements of both Ta/*n*-Si and Ta/*p*-Si executed at room temperature are shown in Fig. 1a and b. As shown in the figures, Ta/*n*-Si and Ta/*p*-Si Schottky diodes have well rectifying properties. Therefore, the simple thermionic emission theory (TET) can be used to obtain electrical properties of Ta/Si diodes. When the TET is taken into account, the current can be expressed as [14]

$$I = I_0 \exp\left(\frac{q(V - IR_s)}{nkT}\right) \tag{1}$$

where q is the electron charge, V is the applied voltage, R_s is the series resistance, n is the dimensionless ideality factor, k is the Boltzmann constant, T is the absolute temperature and I_0 is the saturation current given as;

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \tag{2}$$

with A is the diode area, A^* is the Richardson constant which is equals to 30 and 110 A cm^{-2} K^{-2} for *p*-Si and *n*-Si [15], respectively, and ϕ_b is the Schottky barrier height (SBH). The MS interfaces are an essential part of virtually all semiconductor electronic and optoelectronic devices. One of the most interesting properties of a MS interface is its SBH which is a measure of the mismatch of the energy levels for majority carriers across the MS interface. The SBH controls the electronic transport across MS interfaces and is, therefore, of vital importance to the successful operation of any semiconductor device [1–4,14,16].

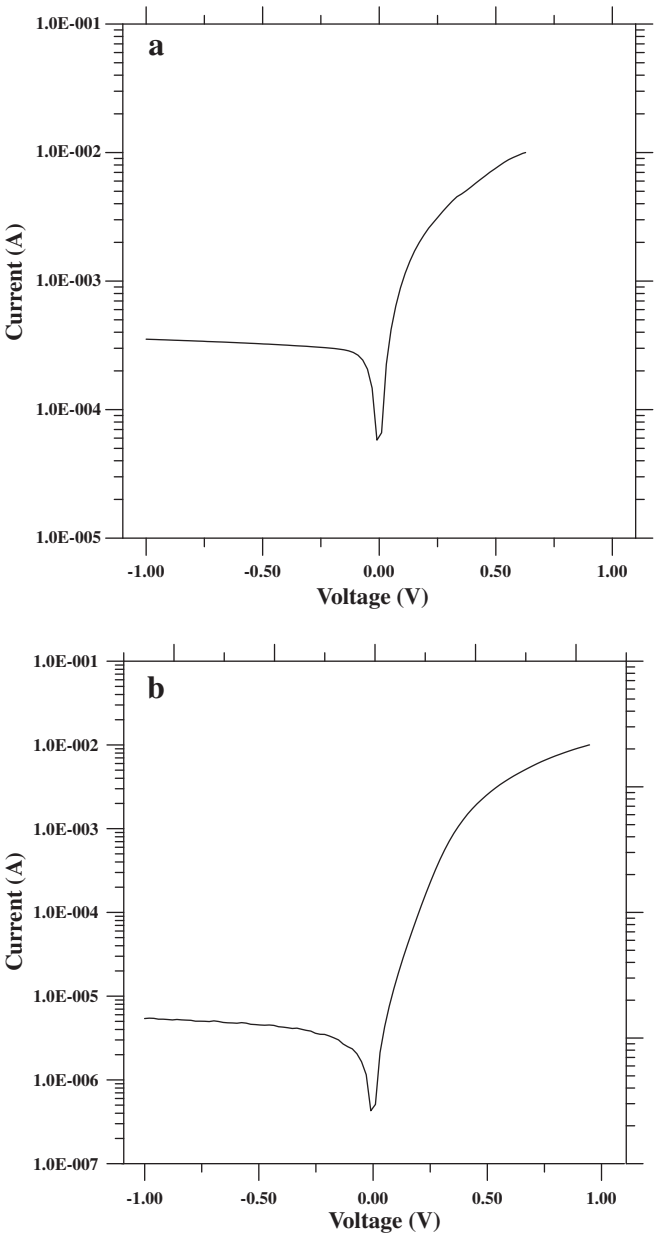

Fig. 1. Current–voltage characteristics of (a) Ta/*n*-Si and (b) Ta/*p*-Si Schottky diodes.

The ideality factor value of a device can be determined from the slope of the linear region of ln *I*–*V* curve using equation through

$$n = \frac{q}{kT}\frac{dV}{d\ln(I)} \tag{3}$$

If the ideality factor n is greater than unity, it implies the deviation from ideal diode [16,17]. That is, the ideality factor is introduced to take into account the deviation of the experimental *I*–*V* data from the ideal thermionic model and should be $n = 1$ for an ideal contact. The ideality factors of Ta/*n*-Si and Ta/*p*-Si Schottky diodes have been calculated as 1.25 and 1.15, respectively. The obtained results from *I*–*V* measurements are also shown in Table 1. The deviation from ideal diode might be due to the effects of native thin oxide layer and the interface states between the metal and the semiconductor. These values of n indicate that the device obey a metal–interface layer–semiconductor (MIS) configuration rather than ideal Schottky diode.

Table 1
Some electrical parameters obtained from *I–V* measurements for Ta/Si diodes.

	ln *I–V*		*dV*/*d*(ln *I*)–*I*		*H*(*I*)–*I*	
	n	ϕ_b (eV)	*n*	R_s (Ω)	ϕ_b (eV)	R_s (Ω)
Ta/*n*-Si	1.25	0.56	1.17	138	0.58	141
Ta/*p*-Si	1.15	0.65	1.58	68	0.74	52

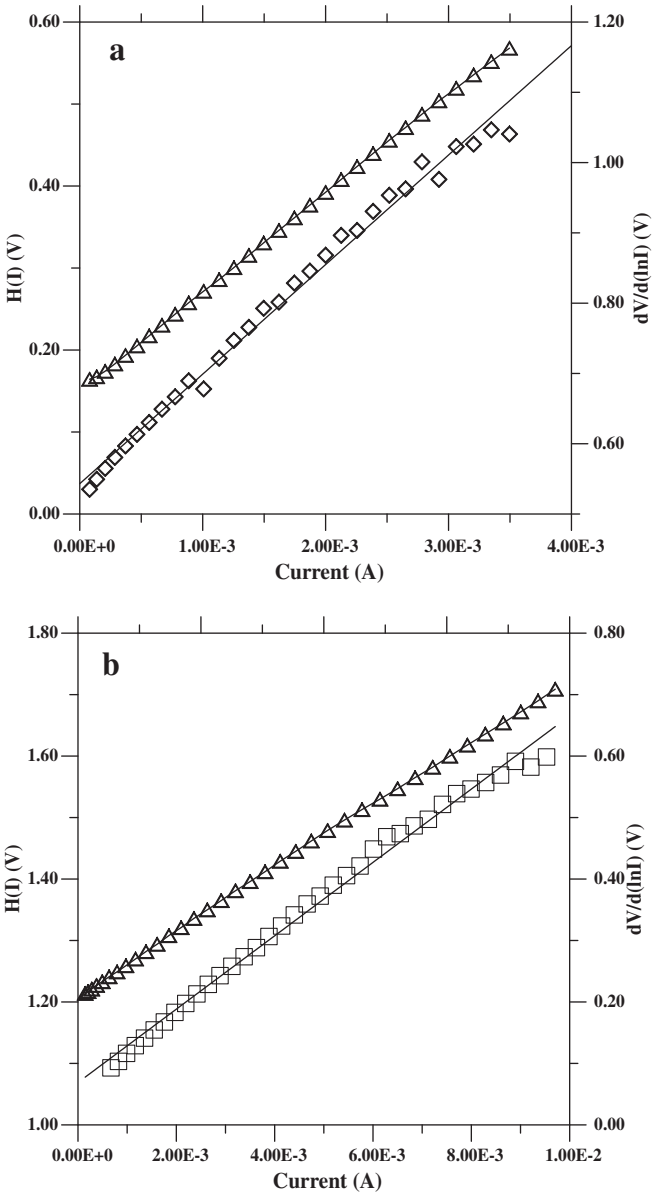

Fig. 2. *H*(*I*)–*I* (triangular) and *dV*/*d*(ln *I*)–*I* (rectangular) plots of (a) Ta/*n*-Si and (b) a Ta/*p*-Si Schottky diodes.

The value of 1.25 or 1.15 for *n* usually leads to films of thickness of the order of 15–20 Å [14]. If Si surfaces are prepared by the usual polishing and chemical etching, and the evaporation of metal is carried out in a conventional vacuum system having a pressure of around 10^{-5} Torr, the Si surface is inevitably covered with a thin insulating film. The native oxide layers can be also formed by water or vapour adsorbed onto the surface of the semiconductor before insertion in the vacuum system. The MS contacts formed under these conditions are not intimate contact because an interfacial oxide layer of atomic dimensions inevitably separates them [1–4,14]. The values of this

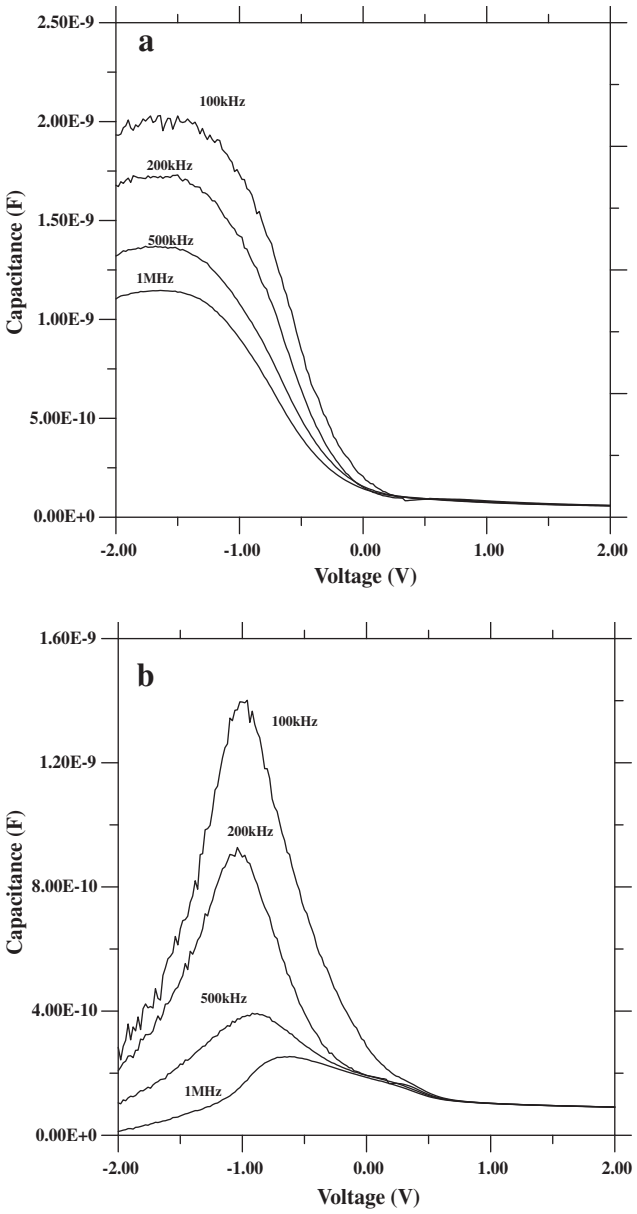

Fig. 3. Capacitance–voltage characteristics of (a) Ta/*n*-Si and (b) Ta/*p*-Si Schottky diodes.

oxide layer thickness are between 10 and 30 Å depending on the method of surface preparation. For a sufficiently thick interface layer, the interface states are in equilibrium with the semiconductor and they cannot interact with the metal [1–4,14]. Therefore, the value dielectric constant ε_i of the interfacial layer should not be very different from the value for bulk SiO_2 [1–4,14].

In addition, ϕ_b values can be calculated using I_0 values determined from the intercepts of ln *I–V* plots on *I* axis using the equation given as

$$\phi_b = \frac{kT}{q} \ln\left(\frac{AA^*T^2}{I_0}\right). \tag{4}$$

The ϕ_b values Ta/*n*-Si and Ta/*p*-Si Schottky diodes have been determined as 0.56 and 0.65 eV, respectively. It is well known that the barrier height value of a Schottky diode is almost metal independent and the sum of the barrier height values ($\phi_{bn} + \phi_{bp}$) for a metal on *p*- and *n*-type semiconductor is equal to the energy gap of semiconductor [18]. However, the sum of calculated barrier heights

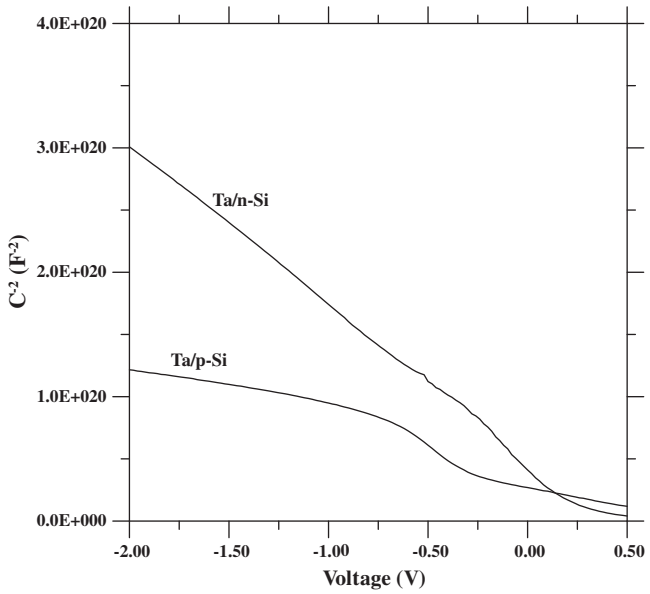

Fig. 4. C^{-2}–V characteristics of a Ta/n-Si and Ta/p-Si Schottky diodes at 500 kHz.

(1.21 eV) for Ta/n-Si and Ta/p-Si is higher than the band gap of the Si (1.12 eV). As mentioned above, it is well known that most semiconductor surfaces are easily oxide when left in air for extended periods of time. A layer of surface oxide or some other contaminant may be present at most semiconductor surfaces, and can significantly affect the SBH of MS interfaces formed on such a surface [1–4,14]. The SBHs formed on the etched surface were sometimes found to differ significantly by ~0.2 eV [14,19]. However, the increase in the sum of the barrier heights may because of barrier height inhomogenity between the metal and the semiconductor Si. According to Song et al. [20], the barrier inhomogeneities can occur as a result of inhomogeneities in the interfacial oxide layer composition, non-uniformity of the interfacial charges and interfacial oxide layer thickness. Therefore it can be claimed that the defects formed during sputtering process have caused inhomogeneities at interface and alter the barrier heights of the diodes. Furthermore, in practice, the barrier height may increase due to the existence of an interfacial layer and the interface states when a forward bias is applied so that the current increases less rapidly with bias [14].

As shown in Fig. 1, the I–V plots deviate from linearity at high voltages. These deviations imply the effects of the interface states and the bulk resistance. The series resistance R_s and n can be determined using the method improved by Cheung and Cheung. The method can be performed using the equations [21]

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right) \tag{5}$$

and

$$H(I) = V - \left(\frac{nkT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) = IR_s + n\phi_b. \tag{6}$$

The plots of $dV/d(\ln I)$–I and $H(I)$–I for both diodes are shown in Figs. 2 and 3. All plots give straight lines in series resistance region as expected. The R_s and $n(kT/q)$ values are determined from the slope and y-axis intercept of the graph $dV/d(\ln I)$–I, respectively. Similarly, the R_s and ϕ_b values are obtained from the slope and y-axis intercept of the $H(I)$–I graph, respectively. The series resistances obtained from both $dV/d(\ln I)$–I and $H(I)$–I plots are used to check the consistency of the method. The obtained results are shown in Table 1. As presented in the table, the R_s values were calculated as 138 and 141 Ω (for Ta/n-Si) and 68 and 52 Ω (for Ta/p-Si). The results show the consistency of the method.

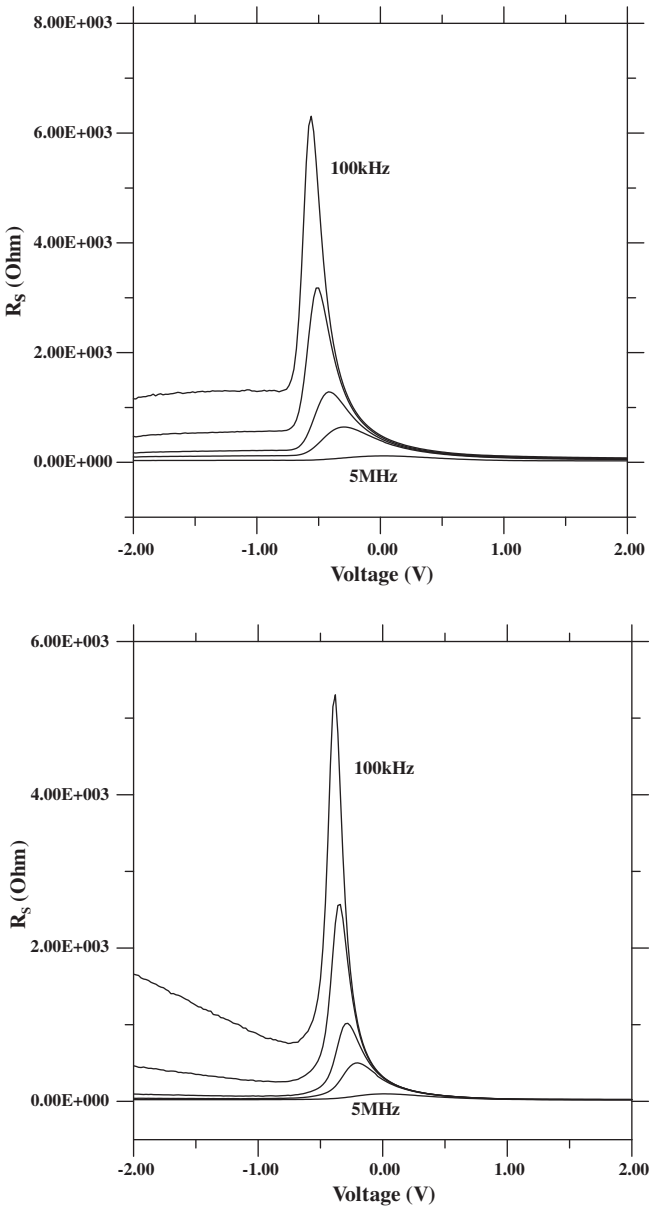

Fig. 5. Series resistance–voltage characteristics of (a) Ta/n-Si and (b) Ta/p-Si Schottky diode at different frequencies (100, 200, 500 kHz, 1 and 5 MHz).

The capacitance–voltage (C–V) characteristics are one of the fundamental properties of Schottky diodes. The C–V plots at different frequencies (100, 200, 500 kHz and 1 MHz) for Ta/n-Si and Ta/p-Si Schottky diodes are shown in Fig. 3a and b, respectively. It is well known that the C–V characteristics of Schottky barrier diodes are extremely sensitive to interface states [1]. As seen in Fig. 3a, while the C–V plots of Ta/n-Si diode has no peaks; Ta/p-Si diode has peaks for all frequencies. The peak value decreases while frequency increases. Therefore, it can be said that the interface states at Ta/p-Si Schottky diodes have a strong effects on electrical properties of the device. In addition, the increase of the capacitance of the device at low frequencies depends on the ability of the electron concentration to follow the applied ac signal. If the C–V measurement carries out at sufficiently high frequencies, the charge at the interface cannot follow an ac signal. These situations are clearly presented in Fig. 3a and b.

The characteristic parameters of the diodes can be also calculated by C^{-2}–V plots. In order to determine the barrier height values of the diodes, the C^{-2}–V graphs are plotted in Fig. 4. The

depletion region capacitance is written for metal/*p*-Si diodes as [22–24]

$$\frac{1}{C^2} = \frac{2(V_{do} + V)}{q\varepsilon_s A^2 N_a} \tag{7}$$

and metal/*n*-Si diodes as [14,25]

$$\frac{1}{C^2} = \frac{2(V_{do} + V)}{q\varepsilon_s A^2 N_d} \tag{8}$$

where A is the effective diode area, ε_s is the dielectric constant of semiconductor and V_d is the diffusion potential at zero bias determined from the extrapolation of the linear reverse bias C^{-2}–V plot to the V axis. The barrier height value can be determined from the relation

$$\phi_b(C{-}V) = V_{do} + V_p \tag{9}$$

where V_p is the potential difference between the top of the valance band in the neutral region of *p*-Si and the Fermi level, and the difference between the bottom of the conduction band in the neutral region of *n*-Si and the Fermi level. The V_p values for *p*-Si and *n*-Si can be calculated when the carrier concentrations N_a and N_d are known. The values of V_p have been calculated as 0.228 eV [26] and 0.279 eV [17] for *p*-Si and *n*-Si semiconductors. The diffusion potential values of 0.54 and 0.41 eV obtained for the Ta/*p*-Si and *n*-Si diodes. Therefore, the barrier height values were 0.77 and 0.69 eV calculated as using Eq. (9). There is a discrepancy between the results obtained from I–V to C–V plots. This discrepancy may be because of the thin native oxide between the metal and the semiconductors. The existence of barrier height inhomogeneity can be another explanation [27].

To see the effects of interface states on electrical properties of the diodes, the R_s–V measurements of the diode have been taken for several frequencies and presented in Fig. 5a and b. Peaks are observed in figures. These peaks are also associated with the interface states [14,28]. The peak intensity is reduced with increasing frequency, confirming that the distribution of density of interface states varies from lower to higher frequencies. The peak was nearly disappeared for 5 MHz. This indicates that the interface states can not follow fast alternating current signal.

4. Conclusions

In conclusion, Ta/Si Schottky diodes have been fabricated by sputtering of tantalum metal on *n*-Si and *p*-Si substrates. The ideality factor, barrier height and series resistance values have been calculated from I–V measurements. The obtained results have been compared from ones determined from C–V measurements. It has seen that the diodes deviate from an ideal diode. This deviation have been attributed the effects of both native oxide layer and the interface state density between the metal (Ta) and the semiconductor (Si). The effects of interface states have been clearly observed in the measurements of both C–V and R_s–V measurements.

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